WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:

a memory cell array;

an address buffer which receives an address signal that indicates an address of the memory cell array;

a latch circuit which latches the address signal output from the address buffer;

an address transition detection circuit which detects transition of the address signal latched by the latch circuit upon receiving an address different from that latched by the latch circuit; and

a control circuit which comprises a timeout circuit that controls a cycle operation of the memory cell array, controls operations of the address buffer and the latch circuit, causes the latch circuit to latch an address at operation start time, which is output from the address buffer, during the operation of the memory cell array, when the address transition detection circuit detects the transition of the address during the cycle operation, causes the latch circuit to latch, after an end of the operation of the memory cell array, an address that is currently input to the address buffer, and controls to execute the next cycle operation of the memory cell array in accordance with the address latched by the latch circuit.

2. The device according to claim 1, wherein the

address buffer is activated immediately before the start of the operation of the memory cell array under control of the control circuit and inactivated during the operation of the memory cell array after the address is latched by the latch circuit.

3. The device according to claim 2, wherein the activation/inactivation of the address buffer is controlled by supplying/cutting off a power.

4. The device according to claim 1, which further comprises a switch which is inserted between the address buffer and the latch circuit and ON/OFF-controlled by a first control signal output from the control circuit, and

in which the address buffer and the latch circuit are set in a connected/disconnected state in accordance with the ON/OFF state of the switch.

5. The device according to claim 4, wherein the address transition detection circuit detects the transition of the address in a state in which the switch is turned off to disconnect the address buffer from the latch circuit.

6. The device according to claim 1, wherein the latch circuit comprises a first latch section which latches the output signal from the address buffer in response to a second control signal output from the control circuit, and a second latch section which latches an output signal from the first latch section

and generates a complementary signal in response to a third control signal output from the control circuit.

7. The device according to claim 6, wherein the address transition detection circuit detects the transition of the address on the basis of the output signal from the first latch section.

8. The device according to claim 1, wherein the memory cell array is constituted by arraying ferroelectric cells in a matrix.

9. The device according to claim 1, wherein the memory cell array is constituted by arraying TC parallel unit series-connected ferroelectric cells in a matrix.

10. The device according to claim 1, wherein the memory cell array is constituted by arraying dynamic cells in a matrix.

11. A semiconductor integrated circuit device comprising:

a memory cell array;

a row address buffer which receives a row address signal that indicates a row address of the memory cell array;

a column address buffer which receives a column address signal that indicates a column address of the memory cell array;

a CE buffer which receives an external chip enable signal;

a WE buffer which receives an external write enable signal;

a first row address latch which latches the row address signal output from the row address buffer;

a second row address latch which latches the row address signal output from the first row address latch and outputs an internal row address signal;

a first column address latch which latches the column address signal output from the column address buffer;

a second column address latch which latches the column address signal output from the first column address latch and outputs an internal column address signal;

a row address transition detection circuit which detects transition of the row address signal output from the first row address latch;

a column address transition detection circuit which detects transition of the column address signal output from the first column address latch;

a chip enable transition detection circuit which detects transition of the external chip enable signal output from the CE buffer;

a write enable transition detection circuit which detects transition of the external write enable signal output from the WE buffer;

an ATD AND circuit which ANDs detection results

from the row address transition detection circuit, the column address transition detection circuit, the chip enable transition detection circuit, and the write enable transition detection circuit; and

an internal CE control circuit which comprises a timeout circuit that controls a cycle operation of the memory cell array, controls a row system circuit and a column system circuit to access the memory cell array and also controls the row address buffer, the column address buffer, the first and second row address latches, and the first and second column address latches on the basis of an AND signal output from the ATD AND circuit, causes the first and second row address latches and the first and second column address latches to respectively latch a row address and a column address at operation start time, which are output from the row address buffer and the column address buffer, during the operation of the memory cell array, and when the row address transition detection circuit detects the transition of the row address or the column address transition detection circuit detects the transition of the column address during the cycle operation, causes the second row address latch and the second column address latch to respectively latch, after an end of the operation of the memory cell array, a row address and a column address that are currently latched by the first row address latch and the first

column address latch so as to control access to the memory cell array.

12. The device according to claim 11, wherein the row address buffer and the column address buffer are activated immediately before the start of the operation of the memory cell array under control of the internal CE control circuit and inactivated during the operation of the memory cell array after the row address signal and the column address signal are latched by the first row address latch and the first column address latch.

13. The device according to claim 12, wherein the activation/inactivation of the row address buffer and the column address buffer is controlled by controlling power on/off in response to a first control signal output from the internal CE control circuit.

14. The device according to claim 11, which further comprises a first switch which is arranged on an input side of the first row address latch and ON/OFF-controlled by a first control signal output from the internal CE control circuit, and a second switch which is arranged on an input side of the first column address latch and ON/OFF-controlled by the first control signal output from the internal CE control circuit, and

in which the row address buffer and the first row address latch are set in a connected/disconnected state in accordance with the ON/OFF state of the first

switch, and the column address buffer and the first column address latch are set in a connected/ disconnected state in accordance with the ON/OFF state of the second switch.

15. The device according to claim 14, wherein the row address transition detection circuit and the column address transition detection circuit detect the transitions of the row address and the column address in a state in which the first and second switches are turned off to disconnect the row address buffer from the first row address latch and disconnect the column address buffer from the first column address latch.

16. The device according to claim 11, wherein the second row address latch supplies, to the row system circuit, the internal row address signal in response to a second control signal output from the CE control circuit, and the second column address latch supplies, to the column system circuit, the internal column address signal in response to the second control signal output from the CE control circuit.

17. The device according to claim 11, wherein the memory cell array is constituted by arraying ferroelectric cells in a matrix.

18. The device according to claim 11, wherein the memory cell array is constituted by arraying TC parallel unit series-connected ferroelectric cells in a matrix.

19. The device according to claim 11, wherein the memory cell array is constituted by arraying dynamic cells in a matrix.

20. An access method for a semiconductor integrated circuit device including a memory cell array, an address buffer which receives an address signal that indicates an address of the memory cell array, a latch circuit which latches the address output from the address buffer, an address transition detection circuit which detects transition of the address, and a control circuit which comprises a timeout circuit that controls a cycle operation of the memory cell array on the basis of a detection result from the address transition detection circuit, comprising:

causing the latch circuit to latch an address at operation start time during the operation of the memory cell array;

causing the address transition detection circuit to detect the transition of the address during the cycle operation;

when the transition of the address is detected, causing the latch circuit to latch, after an end of the operation of the memory cell array, an address that is currently input to the address buffer; and

executing the next cycle operation of the memory cell array in accordance with the address latched by

the latch circuit.

21. An access method for a semiconductor integrated circuit device including a memory cell array, a row address buffer which receives a row address signal that indicates a row address of the memory cell array, a column address buffer which receives a column address signal that indicates a column address of the memory cell array, a CE buffer which receives an external chip enable signal, a WE buffer which receives an external write enable signal, a first row address latch which latches the row address signal output from the row address buffer, a second row address latch which latches the row address signal output from the first row address latch and outputs an internal row address signal, a first column address latch which latches the column address signal output from the column address buffer, a second column address latch which latches the column address signal output from the first column address latch and outputs an internal column address signal, a row address transition detection circuit which detects transition of the row address signal output from the first row address latch, a column address transition detection circuit which detects transition of the column address signal output from the first column address latch, a chip enable transition detection circuit which detects transition of the external chip enable signal output

from the CE buffer, a write enable transition detection circuit which detects transition of the external write enable signal output from the WE buffer, an ATD AND circuit which ANDs detection results from the row address transition detection circuit, the column address transition detection circuit, the chip enable transition detection circuit, and the write enable transition detection circuit, and an internal CE control circuit which comprises a timeout circuit that controls a cycle operation of the memory cell array, controls a row system circuit and a column system circuit to access the memory cell array, and also controls the row address buffer, the column address buffer, the first and second row address latches, and the first and second column address latches on the basis of an AND signal output from the ATD AND circuit, comprising:

causing the first and second row address latches and the first and second column address latches to respectively latch a row address and a column address at operation start time, which are output from the row address buffer and the column address buffer, during the operation of the memory cell array;

causing the row address transition detection circuit to detect the transition of the row address or causing the column address transition detection circuit to detect the transition of the column address during

the cycle operation;

when the transition of the row address or column address is detected, causing the second row address latch and the second column address latch to respectively latch, after an end of the operation of the memory cell array, a row address and a column address that are currently latched by the first row address latch and the first column address latch; and

executing the next cycle operation of the memory cell array in accordance with the addresses latched by the second row address latch and the second column address latch.